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IS MacKenzie - 1999 - yorku.ca
... Modes of Operation; 8-Bit **Shift Register** (Mode 0); ... Mode 3); Initialization and Accessing Serial Port **Register**; ... Hardware **Emulation**; Execution from **RAM**; Execution from ...
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A hardware emulator for binary neural networks
M Skubiszewski - 1990 International Neural Network Conference - citeseer.csail.mit.edu
... carry **register** Partial sum **register** (**shift register**) inputs weights AND output (sign bit of the partial sum **register**) clear ... data **RAM** (with format con- verters) ...
Cited by 9 - View as HTML - Web Search

Emulation of the Sparcle microprocessor with the MIT Virtual Wires **emulation** system
M Dahl, J Babb, R Tessier, S Hanono, D Hoki, A ... - FPGAs for Custom Computing Machines, 1994. Proceedings. IEEE ..., 1994 - ieeexplore.ieee.org
... The gated **shift register** architecture using the I/O pad ... Clock Speed 33 MHz 24 MHz **Emulation** Clock Speed ... High-level structures such as **RAM** are replaced with ...
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ICEBERG: an embedded in-circuit emulator synthesizer for microcontrollers - group of 10 »
J Huang, TA Lu - Proceedings of the 36th ACM/IEEE conference on Design ..., 1999 - portal.acm.org
... circuits, A/D and D/A converters, **RAM**, ROM, I ... be mapped to a machine state in the FPGA **emulation**. ... chain **register** is a multiple-bit **shift- register** consisting of ...
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Exploiting circuit **emulation** for fast hardness evaluation - group of 3 »
P Civera, L Macchiarulo, M Rebaudengo, MS Reorda, ... - Nuclear Science, IEEE Transactions on, 2001 - ieeexplore.ieee.org
... protocol is half-duplex; as a result, two **shift** operations of ... we described in this paper and a **register** transfer (RT ... at 300 MHz and equipped with 256 MB of **RAM**. ...
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Fine-grain system architectures for systolic **emulation** of neuralalgorithms
U Ramacher, W Raab - Application Specific Array Processors, 1990. Proceedings of ..., 1990 - ieeexplore.ieee.org
... Systolic **Emulation** of Neural Algorithms There exist various ways to implement formula (1 ... The 4-stage input **shift register** of the k-th multiplier is ... **RAM** large ...
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TRACER-fpga: a router for **RAM**-based FPGA's - group of 2 »
CD Chen, YS Lee, ACH Wu, YL Lin - Computer-Aided Design of Integrated Circuits and Systems, ..., 1995 - ieeexplore.ieee.org
... Abstract-We describe a routing method for the design of a class of **RAM**-based field ... It is suitable for low-speed applications such as hardware **emulation**. ...
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A FPGA ASIC communication channel systems emulator
KA Page, PM Chau - ASIC Conference and Exhibit, 1993. Proceedings., Sixth ... - ieeexplore.ieee.org
... Essentially the **emulator** must generate an arbitrary sequence of ... than the length of

Published before October 1997
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1 UMAC: a simulated microprogrammable teaching aid
A. Dunworth, V. Upatising
September 1989 **ACM SIGCSE Bulletin**, Volume 21 Issue 3
Publisher: ACM Press
Full text available: pdf(393.14 KB) Additional Information: full citation, citings, index terms

2 Debugging of behavioral VHDL specifications by source level emulation
Gernot Koch, Udo Kebschull, Wolfgang Rosenstiel
December 1995 **Proceedings of the conference on European design automation**
Publisher: IEEE Computer Society Press
Full text available: pdf(630.04 KB) Additional Information: full citation, references, citings, index terms

3 Am2900 Bipolar Microprocessor family
John R. Mick
September 1975 **Proceedings of the 8th annual workshop on Microprogramming**
Publisher: ACM Press
Full text available: pdf(529.29 KB) Additional Information: full citation, abstract, citings, index terms

The Am2900 Bipolar Microprocessor family provides LSI building blocks applicable to numerous high-speed system configurations. The building blocks in this family handle the data path signals, the microprogram control functions, the input/output bus interconnections and the interrupt and timing/control requirements applicable to most digital systems. These building blocks are well suited for computer or central processor emulation, peripheral controllers, communications and voice processors, ...

4 Performance evaluation and improvement of a dynamically microprogrammable computer with low-level parallelism
Shinji Tomita, Kiyoshi Shibayama, Toshiaki Kitamura, Hiroshi Hagiwara
November 1980 **ACM SIGMICRO Newsletter , Proceedings of the 13th annual workshop on Microprogramming MICRO 13**, Volume 11 Issue 3-4
Publisher: IEEE Press, ACM Press
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1 Data file management in shift-register memories
Werner E. Kluge
June 1978 **ACM Transactions on Database Systems (TODS)**, Volume 3 Issue 2
Publisher: ACM Press
Full text available: pdf(1.22 MB) Additional Information: full citation, abstract, references, index terms

The paper proposes a shift-register memory, structured as a two-dimensional array of uniform shift-register loops which are linked by flow-steering switches, whose switch control scheme is tailored to perform with great efficiency data management operations on sequentially organized files. The memory operates in a linear input/output mode to perform record insertion, deletion, and relocation on an existing file, and in a sublinear mode for rapid internal file movement to expedite file posit ...

Keywords: LIFO/FIFO operation modes, data transformations, deletion, insertion, management of sequentially organized files, record retrieval, relocation, shift-register memories, updating

2 A VLIW architecture based on shifting register files
H. Fatih Uğurdağ, Christos A. Papachristou
December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**
Publisher: IEEE Computer Society Press
Full text available: pdf(813.08 KB) Additional Information: full citation, references

3 Shift-register code for indexing applications
M. Nadler, A. Sengupta
October 1959 **Communications of the ACM**, Volume 2 Issue 10
Publisher: ACM Press
Full text available: pdf(616.21 KB) Additional Information: full citation, references

4 Register Synthesis for Speculative Computation
Dirk Herrmann, Rolf Ernst
March 1997 **Proceedings of the 1997 European conference on Design and Test**